APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PROCESSOR DEBUG HALT SIGNAL

Abstract of the Invention

When a DEBUG HALT signal is generated in a target processor during a test procedure, a debug halt sync marker is generated in a program counter trace stream. The debug halt sync marker includes a plurality of packets, the packets identifying that the sync marker is the result of a DEBUG HALT signal. The packets also identify the program counter address at the time of the generation of the DEBUG HALT signal and relate the debug halt sync marker to a timing trace stream.